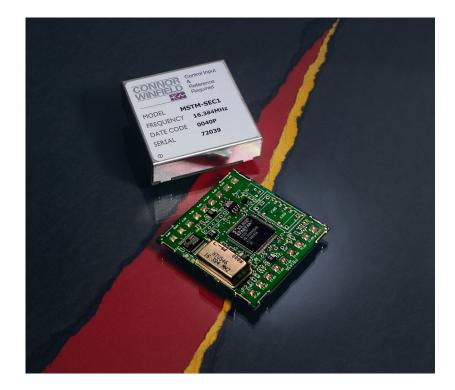
## MSTM-SEC1 Simplified Control Timing Module



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### **General Description**

The Connor-Winfield Stratum SEC1 (SDH Equipment Slave Clock - Option 1) Control Timing Module acts as a complete system clock module for SDH Slave Clock timing applications. The MSTM is designed for external control functions. Full external control input allows for selection and monitoring of any of four possible operating states:

 Holdover; 2) External Reference #1;
External Reference #2; and 4) Free Run. Table 1 illustrates the control signal inputs and corresponding operational states.

In the absence of External Control Inputs (A,B), the MSTM enters the Free Run mode and signals an External Alarm. The MSTM will enter other operating modes upon application of a proper control signal. Mode 1 operation (A=1, B=0) results in an output signal that is phase locked to the External Reference Input #1. Mode 2 operation (A=1, B=1) results in an output signal at or near the frequency as determined by the latest (last) lockedsignal input values and the holdover performance of the MSTM. Free Run ModeFree Run mode operation (A=0, B=0) is a guaranteed output of 4.6 ppm of the nominal frequency.

Alarm signals are generated at the Alarm Output during Holdover and Free Run operation. Alarm Signals are also generated by loss-of-lock, loss of Reference, and a Tune-Limit indication from the PLL. A Tune-Limit alarm signal indicates that the VCXO tuning voltage is approaching within 10% the limits of its lock capability and that the External Reference Input may be erroneous. A high level indicates an alarm condition. Real time indication of the operational mode is available at unique operating mode outputs on pins 1-4.

Control loop filters effectively attenuate any reference jitter and smooth out phase transients.

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# **Absolute Maximum Rating**

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V <sub>cc</sub>	Power Supply Voltage (Vcc to Gnd)	-0.5	-	+7.0	Volts	1.0
V <sub>IN</sub>	Input Voltage with respect to ground	-0.5	-	Vcc+0.5	Volts	1.0
T <sub>STG</sub>	Storage Temperature	-65.0	-	+150	°C	1.0

## Input and Output Characteristics

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V <sub>IH</sub>	High level input voltage (TTL Compatible)	2.0	-	Vcc	V	
V <sub>IL</sub>	Low level input voltage (TTL Compatible)	0	-	0.8	V	
T <sub>IN</sub>	Input signal transition time	-	-	250	nS	
C <sub>IN</sub>	Input capacitance	-	-	15	pF	
C <sub>OUT</sub>	Output capacitance	-	50	-	pF	
V <sub>OH</sub>	High level output voltage @ I <sub>OH</sub> = -8.0 mA, Vcc minimum	2.4	-	-	V	
V <sub>ol</sub>	High level output voltage @ I <sub>oL</sub> = -8.0 mA, Vcc minimum	-	-	0.4	V	
Γ <sub>HL</sub>	Clock out transition time high-to-low, no load	-	4.0	-	nS	
Г <sub>цн</sub>	Clock out transition time low-to-high, no load	-	4.0	-	nS	
Г <sub>RР</sub>	Input 8 kHz reference signal positive pulse width	30	-	-	nS	
T <sub>RN</sub>	Input 8 kHz reference signal negative pulse width	30	-	-	nS	
T <sub>op</sub>	Standard Operating Temperature	0	-	70	°C	

## **Operating Specifications**

Parameter	Specifications	
Frequency Range	16.384 MHz, 19.44 MHz	2.0
Power Supply voltage	5 V <sub>DC</sub> (±5%)	
Supply Current	60 mA Typical at 16.384 MHz	
Timing Reference Inputs	8 kHz	
Jitter and Phase Tolerance	ITU-T G813 7.3	
Wander Generation	ITU-T G813 7.1	
Free Run Accuracy	±4.6 ppm	
Holdover Stability	±0.37 ppm	3.0
Initial Offset	0.05 ppm	
Temperature	2.0 ppm	
Drift	0.01 ppm/day	
Holdover History	40 seconds	
Pull-in / Hold-in Range	±4.6 ppm Minimum	4.0
Lock Time	TBD	
TVL Alarm	1 = WARNING: Reference nearing operational limit	5.0



Table 1

Table 2

Table 3

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## **Control Inputs & Operational States**

Con Inp A	itrol out B		Operational Mode	REF 1	REF 2	Holdover	Free Run	PLL_TVL	Alarm Output
0	0		Free Run (Default)	0	0	0	1	0	1
1	0	External Reference #1	Normal Tune Limit LOR + LOL	1 1 1	0 0 0	0 0 0	0 0 0	0 1 0	0 1 1
0	1	External Reference #2	Normal Tune Limit LOR + LOL	0 0 0	1 1 1	0 0 0	0 0 0	0 1 0	0 1 1
1	1		Holdover	0	0	1	0	0	1

NOTES:

Table 4

1.0 Operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

2.0 Consult factory for other output frequencies.

3.0 Holdover stability is the cumulative fractional frequency offset containing Initial Offset, Temperature, and Drift components as described by ITU-T G.813.

4.0 Pull-in range is the minimum frequency deviation on the reference inputs to the timing module that can be overcome to pull itself into synchronization with the reference.

5.0 A '1' level indicates unit is within the extreme 10% of its operating range tracking the reference (~11ppm). Consult factory for use as a reference qualifier.

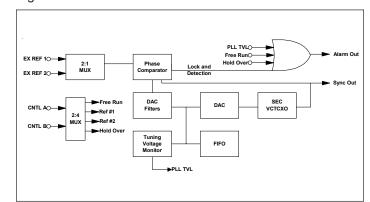
### **Pin Assignment**

Figure 1

+5Vdc	o <b>18</b>	1 0	HOLDOVER
EX REF 1	o <b>17</b>	2 0	REF 1
GND	o 16	3 0	REF 2
EX FEF 2	o <b>15</b>	. 40	FREERUN
GND	o <b>14</b>	5 0	GND
CLK_OUT	o <b>13</b>	6 0	ALARM OUT
GND	o <b>12</b>	7 0	CNTLA
SYNC_OUT	o <b>11</b>	8 0	CNTL B
GND	o <b>10</b>	9 0	PLL TVL

### **Block Diagram**

Figure 2





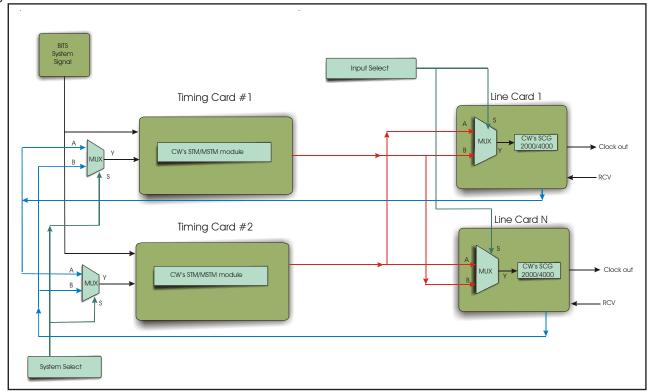
## **Pin Description**

Table 5		
Pin #	Pin Name	Pin Information
1	Holdover	Output. High when the control inputs select Holdover
2	REF 1	Output. High when the control inputs select EX REF 1
3	REF2	Output. High when the control inputs select EX REF2
4	Free Run	Output. High when the control inputs selects Free Run
5	Gnd	Ground
6	Alarm_Out	Output. =1,If (Free Run + Holdover + LOR + LOL + PLL_TVL)
7	Control A	Mode control input
8	Control B	Mode control input
9	PLL_TVL	Tuning Voltage Alarm. =1 If Capture Range Near 10% of Extreme (~11ppm)
10	Gnd	Ground
11	SYNC_OUT	Synchronized output
12	Gnd	Ground
13	N/C	No connection
14	Gnd	Ground
15	Ex REF 2	External Reference #2 Input (8 kHz)
16	Gnd	Ground
17	Ex REF 1	Input. External Reference #1 Input (8 kHz)
18	+5 Vdc	+5 Volt DC supply



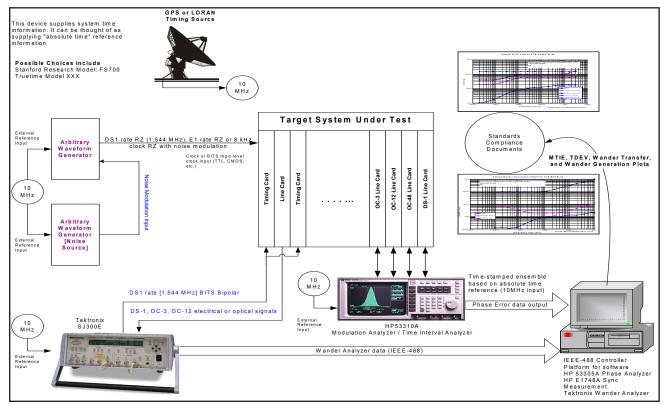
## **Typical Application**

Figure 3



## **Typical System Test Set-up**

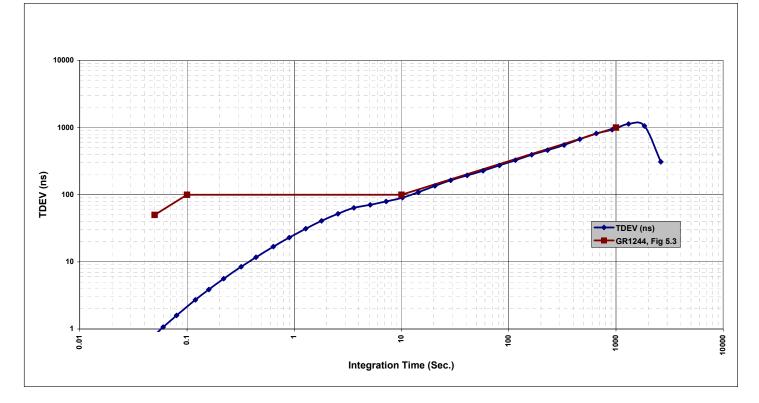
Figure 4





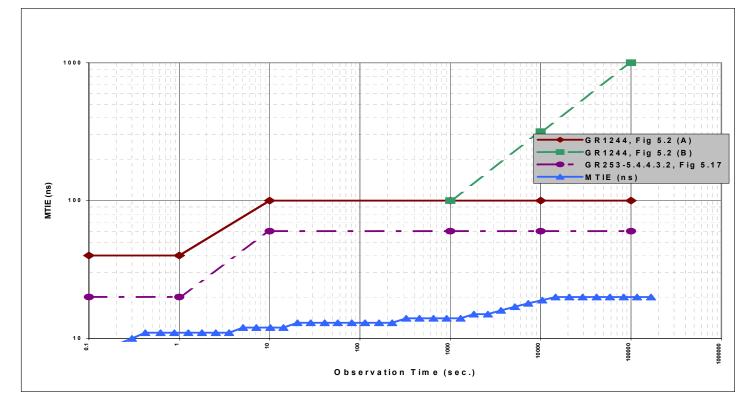
## **Typical Calibrated Wander Transfer TDEV**

Figure 5



# Typical Wander Generation MTIE

Figure 6

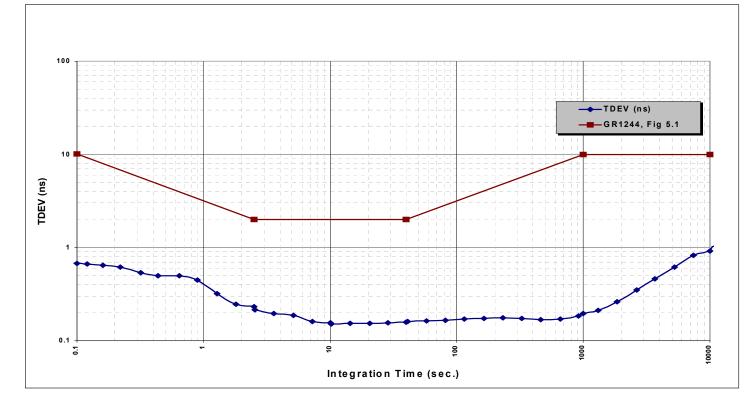




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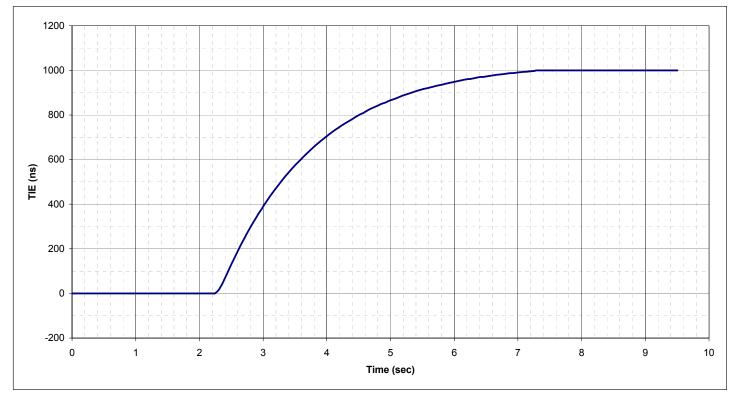
## **Typical Wander Generation TDEV**

Figure 7



## 1µs Phase Transient TIE

Figure 8

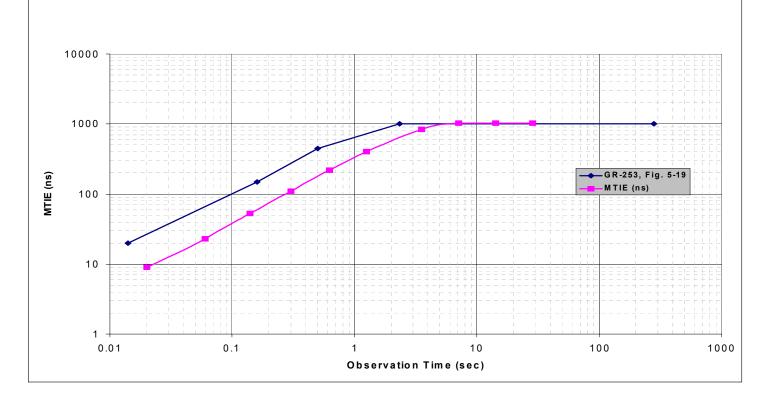




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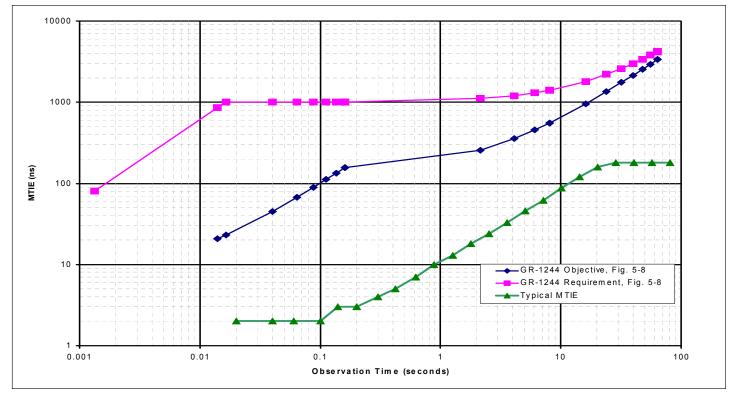
# **Typical Phase Transient MTIE**

Figure 9



## **Entry Into Hold Over**

Figure 10

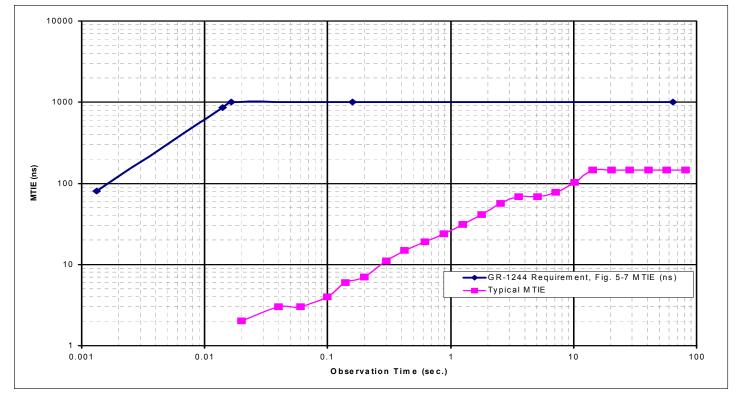




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# **Return from Hold Over**

Figure 11

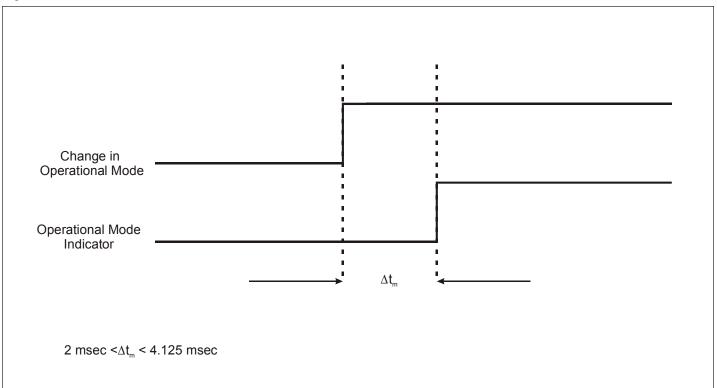




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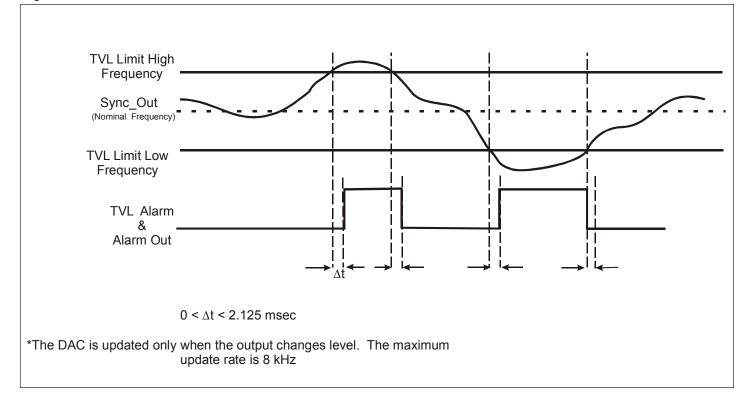
### **MSTM-S3-TR Mode Indicator Delay**

Figure 12



### **Tuning Voltage Limit Alarm Timing Diagram**

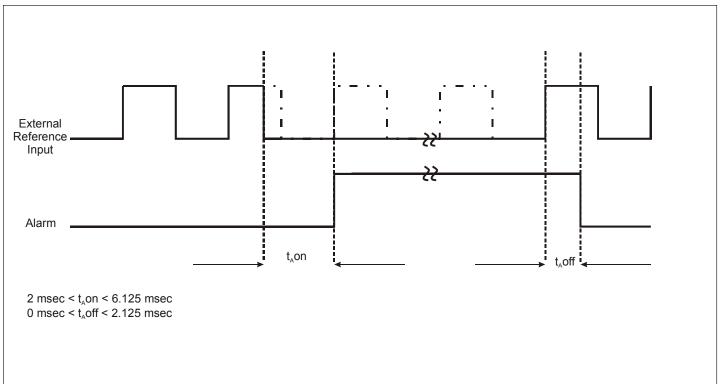
Figure 13





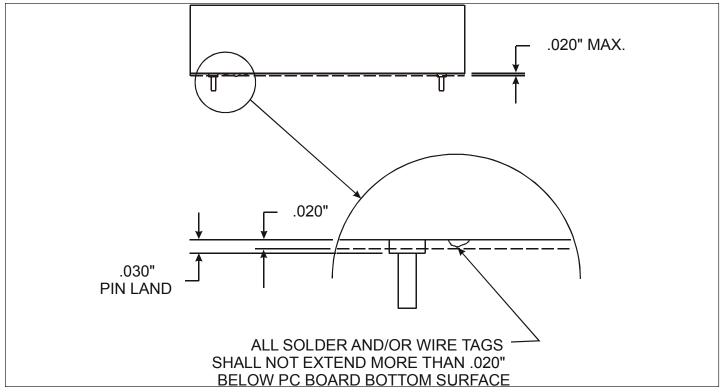
## Loss of Reference Timing Diagram





### **Solder Clearance**

Figure 16





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### **MECHANICAL OUTLINE:**

The mechanical outline of the MSTM-S3-TR is shown in Figure 17. The board space required is 2" x 2". The pins are .040" in diameter and are .150" in length. The unit is spaced off the PCB by .030" shoulders on the pins. Due to the height of the device it is recommended to have heat sensitive devices away where the air flow might not be blocked.

#### PAD ARRAY AND PAD SPACING:

The pins are arranged in a dual-in-line configuration as shown in Figure 16. There is .2" space between the pins in-line and each line is separated by 1.6". See Figures 17 & 18 and Table 6.

#### PAD CONSTRUCTION:

The recommended pad construction is shown in Figure 18. For the pin diameter of .040" a hole diameter of .055" is suggested for ease of insertion and rework. A pad diameter of .150" is also suggested for support. This leaves a spacing of .050" between the pads which is sufficient for most signal lines to pass through.

#### SOLDER MASK:

A solder mask is recommended to cover most the top pad to avoid excessive solder underneath the shoulder of the pin to avoid rework damage. See Table 6 and Figure 19.

#### VIA KEEP OUT AREA:

It is recommended that there be no vias or feed throughs underneath the main body of the module between the pins. It is suggested that the traces in this area be kept to a minimum and protected by a layer of solder mask. See Figure 18.

#### **GROUND AND POWER SUPPLY LINES:**

Power specifications will vary depending primarily on the temperature range. At wider temperature ranges starting at 0 to 70 deg. C., an ovenized oscillator, OCXO, will be incorporated. The turn-on current for an OCXO requires a peak current of about .4A for about a minute. The steady state current will the vary from 50-150 mA depending on the temperature. It is suggested to plan for the peak current in the power and ground traces pin 18 and pin 5. The other four ground pins 10, 12, 14, and 16 are intended for signal grounds.

### **POWER SUPPLY REGULATION:**

Good power supply regulation is recommended for the MSTM-S3-TR The internal oscillators are regulated to operate from 4.75 - 5.25 volts. Large jumps within this range may still produce varying degrees of wander. If the host system is subject to large voltage jumps due to hot-swapping and the like, it is suggested that there be some form of external regulation such as a DC/DC converter.

#### **SOLDERING RECOMMENDATIONS:**

Due to the sensitive nature of this part, hand soldering or wave soldering of the pins is recommended after reflow processes.

#### WASHING RECOMMENDATIONS:

The MSTM-S3-TR is not in a hermetic enclosure. It is recommended that the leads be hand cleaned after soldering. Do not completely immerse the module.

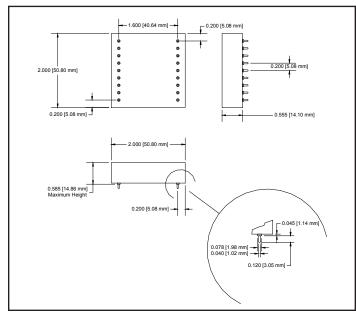
#### MODULE BAKEOUT:

Do not bakeout the MSTM-S3-TR



### **Package Dimensions**

Figure 17

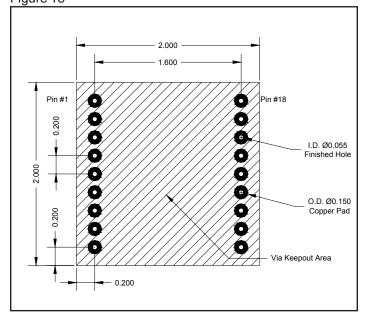


## **Characteristic Measurements**

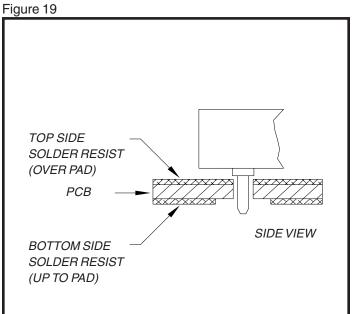
Table 6

Characteristic Item	Measurement (inches)		
Pad to Pad Spacing	0.200		
Solder pad top O.D.	0.150		
Solder pad top I.D.	0.055		
Solder pad bottom O.D.	0.150		
Solder pad bottom I.D.	0.055		
Solder mask top dia.	0.070		
Solder mask bottom dia.	0.155		
Pin row to row spacing	1.600		

### Recommended Footprint Dimensions Figure 18



## Side Assembly View







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Revision	Revision Date Note	
P00	7/27/01	Preliminary Release
P01	8/01/01	Added POR figure and Tri-state pin
P02	9/07/01	Added power supply voltage to Table 3





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